a bit line contact region in the silicon structure adjacent to the other side of the gate electrode;

a first dopant implant in the capacitor and bit line contact regions, the first dopant having a second conductivity type opposite the first conductivity type; and

a second dopant implant in only the capacitor contact region.

24.(new) A device according to Claim 23, wherein the second dopant implant is deeper than the first dopant implant.

25.(new) A device according to Claim 24, wherein the depth of the first dopant implant is in the range of 500 angstroms to 1000 angstroms and the depth of the second dopant implant is up to 2,000 angstroms.

26.(new) A semiconductor memory device, comprising:

a silicon structure having a first conductivity type;

a gate electrode over the silicon structure;

a capacitor contact region in the silicon structure adjacent to one side of the gate electrode;

a bit line contact region in the silicon structure adjacent to the other side of the gate electrode;

a first dopant implant in the capacitor and bit line contact regions, the first dopant having a second conductivity type opposite the first conductivity type;

insulating spacers extending vertically along the sidewalls of the gate electrode and horizontally over a portion of the first dopant implant in the capacitor and bit line contact regions; and

a second dopant implant in only the capacitor contact region.

27.(new) A semiconductor memory device, comprising:

a silicon structure having a first conductivity type;

a gate electrode over the silicon structure having a first conductivity type;

a capacitor contact region in the silicon structure adjacent to one side of the gate electrode;

a bit line contact region in the silicon structure adjacent to the other side of the gate electrode;

a first dopant implant in the capacitor and bit line contact regions, the first dopant having a second conductivity type opposite the first conductivity type;

insulating spacers extending vertically along the sidewalls of the gate electrode and horizontally over a portion of the first dopant implant in the capacitor and bit line contact regions;

a second dopant implant in only the capacitor contact region;

a capacitor first conductor in electrical contact with the capacitor contact region;

a dielectric over the capacitor first conductor; and

a capacitor second conductor over the dielectric.

28.(new) A semiconductor memory device, comprising:

a silicon structure having a first conductivity type;

a gate electrode over the silicon structure;

a capacitor contact region in the silicon structure adjacent to one side of the gate electrode;

a bit line contact region in the silicon structure adjacent to the other side of the gate electrode;

a first dopant implant in the capacitor and bit line contact regions, the first dopant having a second conductivity type opposite the first conductivity type, and the first dopant implanted at a dosage of about 10^{13} ions per square centimeter at an implantation energy in the range of 20 KeV to 100 KeV;

insulating spacers extending vertically along the sidewalls of the gate electrode and horizontally over a portion of the first dopant implant in the capacitor and bit line contact regions;

a second dopant implant in only the capacitor contact, the second dopant implant having the second conductivity type, and the second dopant implanted at a dosage of about 10^{13} ions per square centimeter at an implantation energy up to 200 KeV;

a capacitor first conductor in electrical contact with the capacitor contact region, the capacitor first conductor comprising polysilicon doped to the second conductivity type to a level in the range of 1×10^{19} to 1×10^{20} atoms per cubic centimeter;

a dielectric over the capacitor first conductor; and

a capacitor second conductor over the dielectric.

29.(new) A semiconductor device, comprising:

a silicon structure having first conductivity type;

a gate electrode over the silicon structure;

a capacitor contact region comprising a portion of the silicon structure adjacent to one side of the gate electrode;

a bit line contact region comprising a portion of the silicon structure adjacent to the other side of the gate electrode;

the bit line contact region lightly doped to a second conductivity type opposite the first conductivity type; and

the capacitor contact region heavily doped to the second conductivity type.

Respectfully submitted,

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